which is arbitrarily given. Accordingly, in the system in which the amplitude is fluctuated, the stable adaptive equalization operation can be realized without changing over the reference value for computing the equalization error based on the amplitude. Further, by interlocking the reference value with the threshold value of the binarization circuit which constitutes the rear stage of the equalizer circuit, the equalization characteristics which exhibit the stability to the displacement of the symmetry of the input signal can be realized.

What we claim is

1. An adaptive equalizer circuit which adds given equalization characteristics to signals inputted through a transmission path and performs a control such that an equalization error obtained by performing an arithmetic operation based on an obtained output and a given reference value is minimized thus obtaining equalization characteristics,

the improvement being characterized in that the adaptive equalizer circuit has a constitution to change the equalization characteristics in which the arithmetic operation of the adaptive equalizer circuit is performed in synchronous with a signal having a phase different from the reference clock signal of the signal by a 1/2 clock cycle, and the equalization

characteristics are changed by computing the equalization error based on a first output value after a sign of the output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive and said given reference value.

2. An adaptive equalizer circuit according to claim 1, wherein the constitution to change the equalization characteristics is a constitution in which the equalization characteristics of the adaptive equalizer circuit are changed based on the first output value after the sign of the output of the adaptive equalizer circuit is changed from positive to negative and a first reference value, and the equalization characteristics of the adaptive equalizer circuit are changed based on the first output value after the sign of the output of the adaptive equalizer circuit is changed from negative to positive and a second reference value.

3. An adaptive equalizer circuit according to claim 2, wherein in addition to the change operation of the equalization characteristics of the adaptive equalizer circuit, the adaptive equalizer circuit is constituted such that the equalization characteristics of the adaptive equalizer circuit is changed based on the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative and the second reference value, and the equalization characteristics of the adaptive equalizer circuit is changed based on the output value immediately before the sign

of the output of the adaptive equalizer circuit is changed from negative to positive and the first reference value.

4. An adaptive equalizer circuit according to claim 1, wherein said constitution which changes the equalization characteristics is a constitution in which the equalization characteristics of the adaptive equalizer circuit are changed based on the first output value after the sign of the output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive and the first reference value, and the equalization characteristics of the adaptive equalizer circuit are changed based on the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive and the second reference value.

5. An adaptive equalizer circuit according to claim 2, wherein the second reference value is set to a value which inverts the sign of the first reference value.

6. An adaptive equalizer circuit according to claim 1, wherein the adaptive equalizer circuit is operated to sample an input signal with a signal having a phase different from the reference clock signal which is in synchronous with the input signal by a 1/2 clock cycle, and the equalization characteristics is changed based on the output value of the adaptive equalizer circuit.

7. An adaptive equalizer circuit according to claim 1,

wherein the adaptive equalizer circuit is operated by sampling an input signal with a reference clock signal in synchronous with the input signal and computes an output value of the adaptive equalizer circuit which is in synchronous with a signal having a phase different from the reference clock signal by a 1/2 clock cycle by an interpolation and changes the equalization characteristics of the adaptive equalizer circuit using the computed value.

8. An adaptive equalizer circuit according to claim 1, wherein the reference values are changed corresponding to the change of threshold values at the time of binarizing the output of the adaptive equalizer circuit.

9. An adaptive equalizer circuit according to claim 1, wherein the signals inputted to the adaptive equalizer circuit are signals optically read from a recording medium.